DIL Switch Settings, Links, Options, etc.

There are two positions on the card where DIL switches may be fitted, they are labelled on the diagrams as S1 and S2. DIL switches are now supplied in the standard kit of parts and should be fitted into the DIL sockets provided. (Strangely many designers do not use sockets for DIL switches even though being mechanical components they are more likely to fail than ICs, and every bit as hard to remove once soldered.) It is usually the case that many of the switches are left open so it is quite feasible to fit much smaller DIL switches than the full 16-pin types specified. However, for the purposes of this description it will be assumed that the largest DIL switches have been fitted in each case.

The type of DIL switch to be used is 8 x SPST. It is therefore convenient to refer to the eight switches (for example the S1 pack) as S1a to S1h; oriented so that S1a would connect pins 1 and 16 of the socket, if the pins were counted in the same way as for a 16-pin I.C. Very often the DIL switches themselves are numbered 1-8, corresponding to a-h in this notation. Letters rather than numbers have been chosen because of the potential confusion of referring to say S1-2; it might not be immediately clear whether reference was being made to switch 1 of switch pack 2, or switch pack 1, switch number 2.

DIL Switch S1a-h

The switches S1a-S1h select the I/O Port address. This will have to suit whatever software is in use; the settings for Interak 1 are given at the end of the next paragraph. S1a is the MSD (most significant digit) and corresponds to the chosen state of address bus line AB7; the other switches continue in sequence until S1h is reached, which corresponds to AB0 (the LSD, or least significant digit). Since the DTI-1 card uses two I/O ports i.e. two 256ths of the total number, then only 7 bits can be selected, the switch corresponding to AB0 is a dummy. (7 bits because two 256ths = one 128th, and only seven bits are needed to decode one 128th, since each bit can have one of two states, and 2^7=128.)

Note that due to the fact EX-OR gates are used to select the chosen address (see circuit diagram Sheet 2), the complement of the address should be set on the switches, i.e. for an address with a "1" on a given line, the corresponding switch should be set to "0", by turning that switch ON. For example for use in an Interak 1 system with a ZYMON monitor, the Tape UART Status and Data Ports are 04H and 05H respectively. In binary notation this is 0-0-0-0-0-1-0-X where "X" = "0" for Port 04H and "1" for Port 05H. The required settings for S1a to S1h are therefore OFF-OFF-OFF-OFF-OFF-ON-OFF-X ("X" = "don't care").

In general only seven switches are ever required, and in this specific case only one switch needs to be closed. There is thus no real need to purchase a full 8 x SPST type, one with less switches will do just as well in this application.

DIL Switch S2a-h

This selects such things as number of stop bits, number of bits transmitted, even/odd parity, and no parity.

The selections will be explained in greater detail in a future issue of this manual. (The future issue will be sent free of charge to all users who have purchased the present document.)

For use in the Interak 1 computer running ZYMON 2, the switch settings are simplicity itself: all S2 switches should be OFF.

Optional Parity Selection.

Although ZYMON 2 (the monitor program for the Interak 1 computer) has its own method of checking for errors, other systems, or indeed a future version of this one, may use the common method of "parity" bit checking. When this is selected, an extra bit, called the "parity" bit, is added to the data stream; the polarity of the parity bit depends on whether the number of "1"s in the data transmitted is "odd" or "even", and also on the type of parity selected (which can be "odd" or "even"):

The parity bit is transmitted after the data bits have been transmitted just before the stop bit or bits. The UART calculates the parity of the data bits and arranges the polarity of the parity bit so that the total number of "1"s transmitted (including the parity bit) is odd if "odd" parity has been selected, and even for "even" parity.

The UART performs a similar calculation on received data, but this time compares the calculated parity with the received parity bit. If a discrepancy is found the "Parity Error" flag is set. With suitable software this flag can be tested and so the program which is in control can detect any single bit error in a group of data bits + parity bit.

Odd parity is often preferred to even parity there will always be at least one logic "1" transmitted: the parity bit would have to be "1" even if the data were all "0"s.

Since ZYMON 2 does not examine the parity error flag, it is immaterial whether parity is selected or not, but those users who are of a conservative disposition may care to make all their recordings now with a parity bit, in case it is ever of some use in the future.

The addition of a parity bit, set for "odd" parity, is achieved by making contacts S2a and S2e ON, using switches or wire links. (S2e OFF means "no parity", ON means "parity"; S2a OFF means "even parity selected", ON means "odd parity selected").

Other Setting Up, Link Selections etc.

The DTI-1 card has been designed so that setting-up is very simple; however there are numerous minor details which certain users may care to alter for their own special purposes, or to recover "difficult" recordings made on other computers, and several of the options available may be of assistance to such users. The majority of users will simply make the standard recommended connections, as summarised below.

Summary of connections P1 - P10

(Fuller details follow this summary)

- P1 Motor ON-AUTO-OFF Front Panel Switch FPS2
- P2 300-1200-2400 Baud rate Front Panel Switch FPS1
- P3 Normally unlinked. (Link 1-2 to obtain 600 baud)
- P4 Front Panel Components relating to CASSETTE 0
- P5 Front Panel Components relating to CASSETTE 1
- P6 Received Data Clock. Normally link 1-2 for phase-locked loop operation, (2-3 for fixed crystal clock).
- P7 Link 1-2 for normal time constant for phase-locked loop. (Make no links for fast response; link 2-3 for special purposes).
- P8 Normally link 1-2 to make conventional CUTS tapes, (link 2-3 for logic inversion).
- P9 Normally link 1-2 to read conventional CUTS tapes, (link 2-3 for logic inversion).
- P10 Make no links for modern 5V-only UARTS (e.g. type 1015), (link 2-3 to connect -12V to pin 2 of older multirail UARTS, e.g. type 1013).

Detailed Description of P1 - P10 links

P1 3-pin assembly for connecting front panel switch FPS2. (OFF-AUTO-ON motor control relays, switch biased centre off).

P1	FPS2	
1	1	(top)
2	2	
3	3	

P2 3-pin assembly for connecting front panel switch FPS1. (300-1200-2400 Baud Rate Selection, three position centre off).

P1	FPS1	
1	1	(top)
2	2	
3	3	

P3 3-pin assembly, not normally connected, but can be used to convert the function of FPS1 temporarily to 1200-600-1200 baud, so that a 600 baud tape can be loaded. To make this conversion link P3 pins 1-2.

P4 7-pin assembly, made up from 1 x 3-pin and 1 x 4-pin, for connecting the front panel components associated with Cassette 0:

P4	Function	Connect to:
1	Motor On LED Indicator	LED0 anode (a)
2	Motor On LED Indicator	LED0 cathode (k/'+')
3	Input from Tape	J0 pin 3
4	Output to Tape	J0 pins 1 and 4
5	Common (0V)	J0 pin 2 and body
6	Relay RLY1	J0 pin 6
7	Relay RLY1	J0 pin 7

P5 7-pin assembly, made up from 1 x 3-pin and 1 x 4-pin, for connecting the front panel components associated with Cassette 1:

P5	Function	Connect to:
1	Motor On LED Indicator	LED1 anode (a)
2	Motor On LED Indicator	LED1 cathode (k/'+')
3	Input from Tape	J1 pin 3
4	Output to Tape	J1 pins 1 and 4
5	Common (0V)	J1 pin 2 and body
6	Relay RLY2	J1 pin 6
7	Relay RLY2	J1 pin 7

P6 3-pin assembly. This controls the signal from which RCP (UART Receive Data Clock) is derived. Normally link P6 pins 1-2 for phase locked loop operation, i.e. the clock synchronised with the data recorded on the tape.

(Alternatively, but not normally, link P6 pins 2-3 so that RCP is derived from the fixed quartz crystal and not the recorded data on tape. This can sometimes give superior results if very bad tape etc. is used, having severe dropouts and speed variations which cause the operating conditions of the phase locked loop to vary excessively in trying unsuccessfully to maintain the locked condition.)

P7 3-pin assembly. This adjusts the time constant of the phase locked loop filter. For normal use link P7 pins 1-2, but with very high quality tape and recorders, where "wow and flutter" and dropouts are less of a problem, no link need be made. This will shorten the time taken for the phase locked loop to achieve the locked condition, and respond to subsequent variations. This reduction could be useful in special circumstances, e.g. if the header has been lost accidentally from a recording.

If it is required to load a tape which is not quite CUTS (e.g. as recorded on the "Kemitron" tape interface, which uses CUTS frequencies, but disregards the timing of the zero crossings), the phase locked loop will have great difficulty in achieving lock. One procedure to follow then is to use crystal control (by linking P6 pins 2-3 as discussed for P6 previously), but alternative procedures can be tried:

(a) Increase the phase locked loop filter time constant still further, by fitting capacitor C26, value chosen by experiment, 22u, 47u, or even larger, and linking P7 pins 2-3. This will damp the phase locked loop circuit so much that it will be forced to settle at the average of the previous extremes, namely the required frequency.

or,

(b) Instead, connect a variable voltage linked to P7 pin 2, (e.g. the wiper of a 1k potentiometer connected between the +5V and 0V rails). This will provide direct control of the voltage controlled oscillator in U13, which can then be adjusted by experiment to the frequency which is best for recovering the data from the non standard tape which it is desired to load.

P8 3-pin assembly. This is normally linked between pins 1 and 2 to record tapes under the normal CUTS convention, i.e.

logic "1" = 2400 Hz audio tone,
logic "0" = 1200 Hz audio tone.

(For the opposite, non-standard, convention, sometimes used intentionally or otherwise in other tape interface designs, link P8 pins 2-3 instead.)

P9 3-pin assembly. This is normally linked between pins 1 and 2 to load tapes recorded under the normal CUTS convention, i.e.

logic "1" = 2400 Hz audio tone,
logic "0" = 1200 Hz audio tone.

(For the opposite, non-standard, convention, sometimes used in other tape interface designs, link P9 pins 2-3 instead.)

P10 3-pin assembly. This provides a means for connecting -12V to pin 2 of the UART, U15. All modern UARTs are single +5V rail devices, and normally therefore no links are made on P10.

(If -12V is required to suit some earlier UART, e.g. type AY-5-1013, link P10 pins 2-3. Pin 2 of the UART is decoupled via C27, already provided on the circuit board; if some function other than -12V, or "no connection", has been adopted on some other, non-standard, UART that you may wish to use, then C27 should be removed.)

RV1, RV2

These two miniature potentiometers control the maximum amplitude of the output signals delivered to CASSETTE 0 and CASSETTE 1 respectively. The normal setting for RV1 and RV2 is fully clockwise. The typical maximum output levels will then be approximately as follows:-

125 mV r.m.s. i.e. 350 mV peak to peak

If these levels are too high for your particular equipment, e.g. if they are connected to, and overload, sensitive inputs intended for microphones, the adjustment screws can be turned anti-clockwise to reduce (attentuate) the signal level.

Generally, however microphone and other very low signal level inputs should be avoided, since the effect of background noise, mains hum etc. will be more significant.

See also the note below the next section.

R18, R20

Normally no resistors are fitted in these positions, but if RV1 and RV2 are habitually used very close to their minimum settings to suit some unusual tape recorder, then R18 and/or R20 can be fitted to provide additional attenuation. For example 100 ohm resistors will reduce the maximum output signal to about one tenth of its previous level (the calculated factor is R18/(R18+R19), e.g. 100/(100+1000) = 0.09).

Note: RV1, RV2, R18, R20

These can all be varied independently, to suit say two different recorders which may be connected to the two available front panel connectors J0 and J1.

R41, R42, R43, C31

In the fairly unlikely event of the output signal being too small to suit the cassette recorders in use, all of these values can be altered. For d.c. R41 and R43 are in series, and bias the transistor Q1 at half the supply voltage, but for a.c. they are effectively in parallel; equivalent resistance =

(R41 x R43)/(R41 + R43), i.e. (10k x 10k)/(10k + 10k) = 5k

In conjunction with R42 (47k) this forms a potential divider which reduces the signal amplitude by 5k/(47k + 5k) = approximately one-tenth.

To increase the amplitude of the signal R41 and R43 can be increased to values up to 100k or more (keep R41 and R43 equal), and/or R42 decreased to 1k. C31 may then need attention so as to keep the wave-form the same as it was previously. This is probably easiest to do by selection on test, as its value depends on the combination of R41, R42, R43 adopted, and is tedious to calculate. (In order to make the correct selection of C31, examine and sketch the the wave-form before any alterations are made.)

N.B. It should be stressed that alteration of these components is only necessary in the most unusual circumstances, and they should normally be left strictly as specified on the parts list.

R37, R40

These conduct the current to the transistors which turn on the motor control relays for CASSETTE 0 and 1 respectively. Normally they are connected in such a way that both relays are ON when power is applied. This is convenient for fast-winding tapes and so on, since the motors are already on. If it is preferred that at power on the relay(s) are OFF then R37 and/or R40 can be fitted in the alternative positions R37a, and R40a respectively. If this is done the front panel switch FPS2 will need to be re-labeled ON-AUTO-OFF, instead of OFF-AUTO-ON, or connections to its terminals 1 and 3 reversed.

The alternate position may be adopted for just one of the resistors, so that for example at power on one of the relays is ON and the other is OFF, (this would need further attention to be paid to the naming of the function of the front panel control switch).

Input signal level to DTI-1 Card

This should be as large as possible, up to around 4 or 5 volts r.m.s. (15 volts peak to peak).

Typically about 1 volt r.m.s. (3 volts peak to peak) is a reasonable signal amplitude, which can be provided by the majority of small portable cassette recorders and hi-fi decks.

If an oscilloscope is available increase the amplitude of the signal until "clipping" occurs at the tops and/or bottoms of the peaks.

With common cheap cassette recorders, the maximum signal is to be obtained from the loud-speaker output. If this is uncomfortably loud an earphone can sometimes be used instead of the loud-speaker and/or a dummy resistor load. Many people prefer to listen to a tape as it is loading, as confirmation that all is well.

With good quality recorders and tape, lower input signal levels to the DTI-1 can be tolerated, perhaps down to a tenth of the normal amplitude specified above. It is strongly recommended however that low signal levels be accepted only as a last resort, as there is then a reduced safety margin to cope with trouble, such as worn patches of tape.

Recorded signal level

If automatic level control is employed, then this is outside the control of the user, who simply has to ensure that the signal level chosen is high enough for the automatic control to cope without recording the background noise caused by too low an input level, but not so high that it overloads the automatic control.

The rule to follow is to make the signal as large as possible, without excessive distortion.

If manual control and a recording level meter are provided on your equipment, use a level higher than the maximum marked on the meter, e.g. +3 dB or more. This is because the signal used for our purposes does not need to be hi-fidelity, it just needs to be loud. Do not increase the level so far that severe distortion appears on the playback signal, nor so far that the erase circuit of the recorder has difficulty in erasing it properly.

Frequency Response

This is largely unimportant, since the 1200 Hz and 2400 Hz tones used are in the centre of the audio band and are very easy to record. It may be noticed that on playback with cheap machines, the amplitude of the 2400 Hz tone is much smaller; perhaps half that of the 1200 Hz tone. This is due to the poor frequency response of cheap recorders. Also it may be noticed that the waveform on playback is quite different to that which was recorded. This is also due in the main to poor frequency response (or perhaps more correctly inadequate attempts to correct it ("specmanship"); if capacitor filters are used in a casual way inside the recorder the frequency response may indeed be improved, but phase distortion may be the undesirable result - a case of the cure being worse than the disease.)

Neither of these effects will cause any difficulty in themselves, since it is the timing of the zero-crossings of the signal which is important, not the signal's size or shape.

Tone Controls

If these are provided, their adjustment will have to be a matter for some experiment. Tone controls should not be adjusted for the "prettiest" wave-form viewed on an oscilloscope, but instead adjusted so that the essential timing information (position of zero crossings) is preserved as accurately as possible.

One suggested method is to record some known data, such as a several K block of 55 hex. and play it back at very reduced amplitudes until several errors regularly appear; tape errors are very easy to see in an Interak system due to the invaluable ZYMON feature which displays data and check-sums while loading is in progress. The tone controls can then be adjusted under these arduous contitions to minimise the number of errors found each time the experiment is repeated, until an optimum setting is found. The playback level should then be restored to normal.

Setting up without any Test Equipment

In order to select the best levels etc. in the absence of test equipment, the general method described in the paragraph immediately above can be followed. If you have a choice of signal amplitude, err on the "loud" side.

"Hum" or "Earth" loops

These are well familiar to designers and users of audio equipment. A proper scientific discussion is very complex, but in essence the terms describe a problem where audible mains freqency interference is superimposed on an audio signal path.

For example, if you had a record player correctly earthed for safety or other reasons, and similarly an audio amplifier, then an "earth loop" is produced when a screened audio signal connection is made

between the two items described. The "earth loop" so produced acts as a shorted turn of an imaginary transformer, which conducts a small mains frequency circulating current which is induced by the mains wiring present in virtually all inhabited buildings.

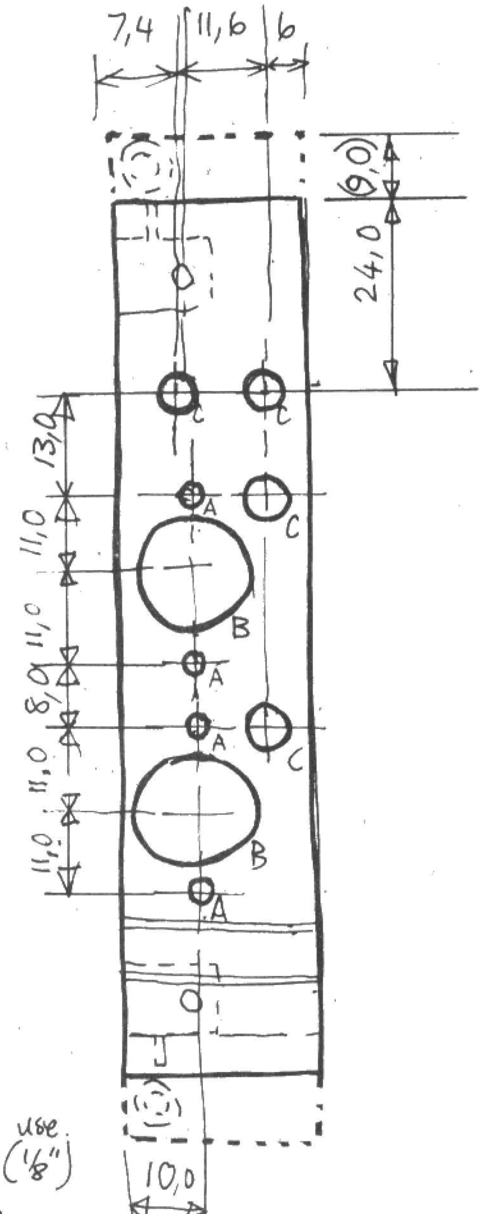
This current generates a very tiny voltage along the length of the earth connection between the two pieces of equipment, but since the amplifier's very purpose is to amplify very tiny voltages at its input, with respect to its own earth, an audible signal at mains frequency is produced.

It is fairly easy to prevent this simply by breaking the earth loop, the main difficulty is to avoid the safety risks sometimes involved in removing the earth connection incorrectly.

A very similar state of affairs exists when connecting one or more cassette recorders to the Interak computer. Screened lead should be used, the screen usually also making common 0V or "earth" connection between the various apparatus. Although "earth loops" can easily occur if the cassette recorder(s) are earthed to the mains earth, this will not necessarily cause a problem if the amplitude of the mains freqency interference is very small in relation to the signals involved. If mains hum is audible, or "visible" on the oscilloscope screen, then the methods adopted in the audio world will have to be considered. Only an experienced audio engineer will be able to feel confident in this area, but in most cases if "earth loops" cause a problem they can most conveniently be broken by removing the earth screen connection inside the audio connector plug(s) which are used for the recorder(s).

If the cassette recorder is battery powered, or has only a two core (i.e. no earth) mains lead, there is no problem of this nature. However a poorly smoothed power supply in the cassette recorder, or inadequately screened audio cables can still cause hum, and any appropriate steps should be taken to eliminate this if it exists.

D.M.P. January 1983
(Revised February 1983 and
March 1984)



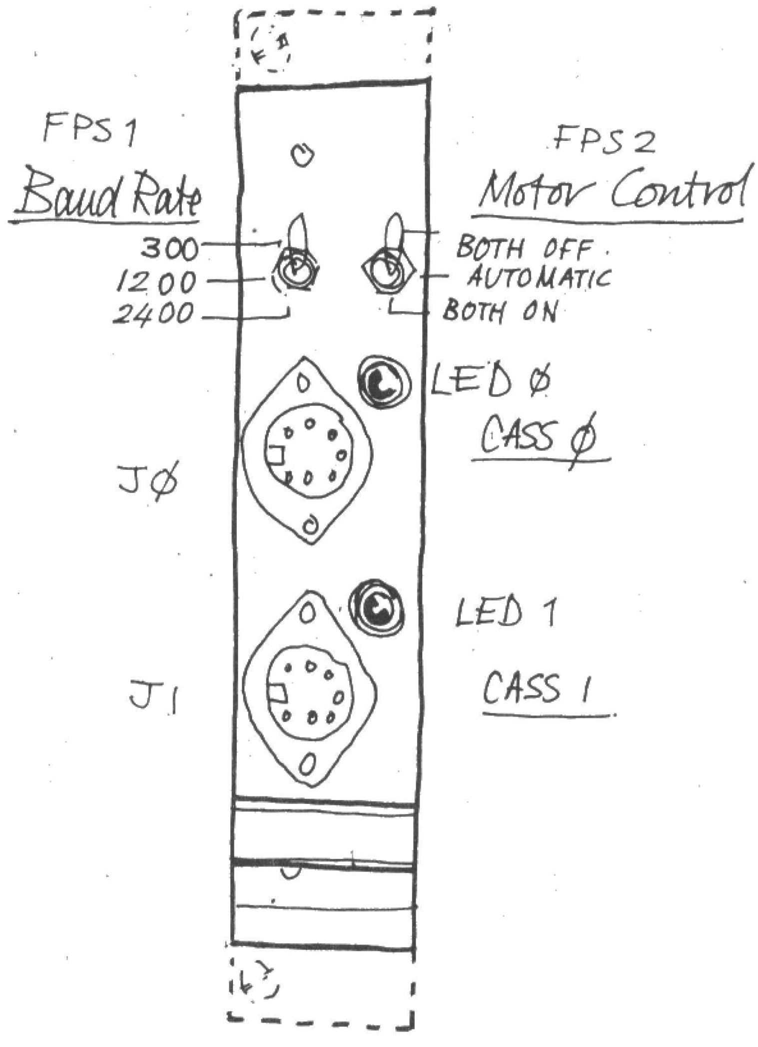
FOUR 'A' HOLES 3,5 dia (use 1/8")
TWO 'B' HOLES 16,0 dia.
FOUR 'C' HOLES 6,35 dia (1/4")

Amended to show new card front dims old card front shown dotted. MAR. 84.

Drwn	DMP
Date	18-5-82
Scale	1:1
Dims	MM

Greenbank Electronics

DTI-1 FRONT PANEL DRILLING



OLD STYLE CARD FRONT SHOWN DOTTED
MAR 84.

Drwn DMP
Date 3-6-82
Scale 1:1

Greenbank Electronics

DTI-1 FRONT PANEL COMPONENTS

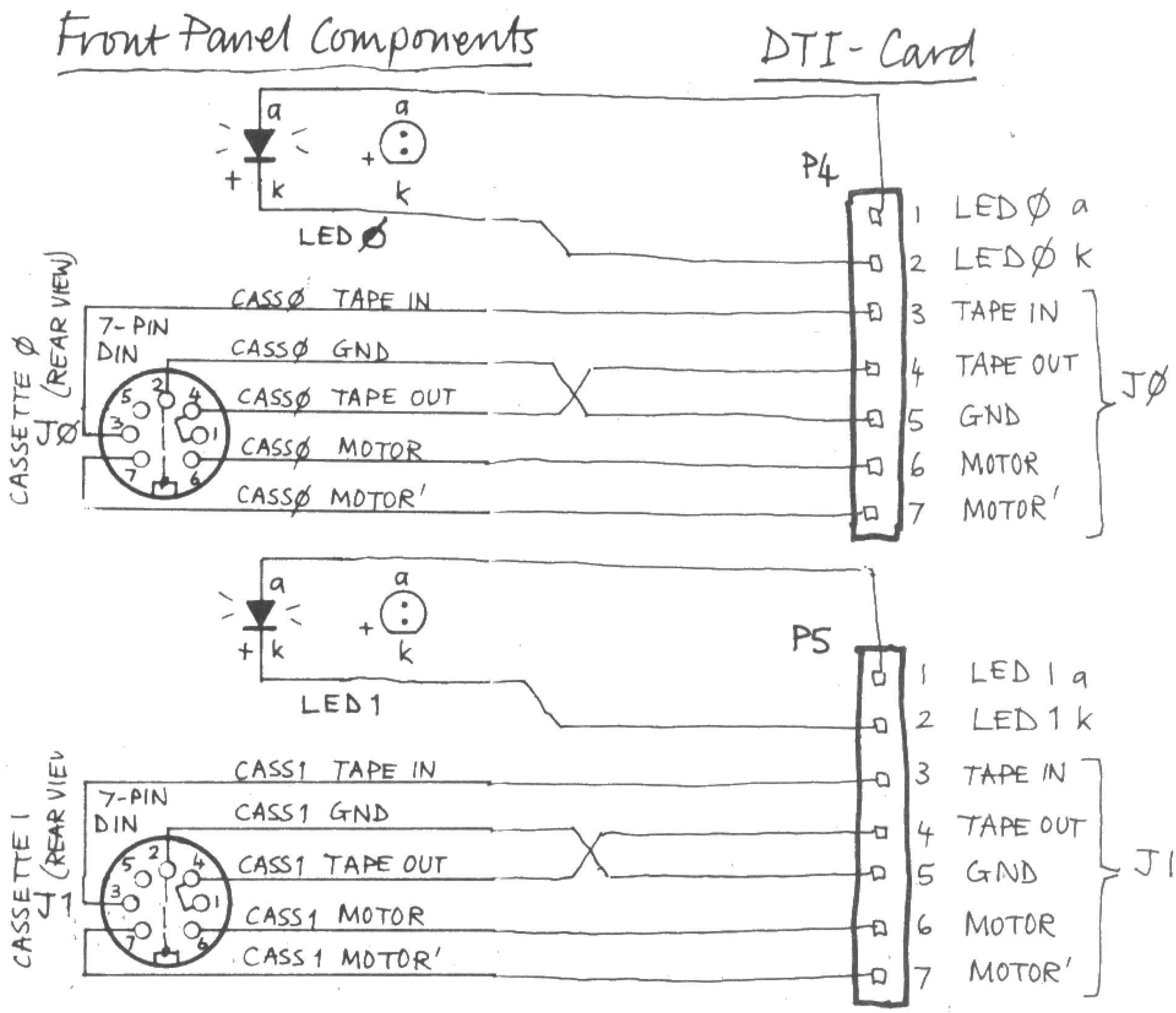
CASSETTE DIN CONNECTORS.

Link output pins 1,4 at the rear of the sockets (this provides an output to both left and right-hand channels of a stereo tape cassette machine).

The input to the computer is taken via pin 3 from the left -hand channel output of a stereo cassette machine. Pin 3 is also the connection for a mono machine, or a stereo machine which is switched to mono output.

Pins 3 and 5 are not linked here, in case this would damage a stereo tape recorder by shorting its left and right-hand channels together; generally, this action is carried out inside a stereo cassette machine when it is switched to mono.

When a stereo cassette machine is in use, it should preferably be switched to mono.



Amended, tape in pin 3, MAR 84.

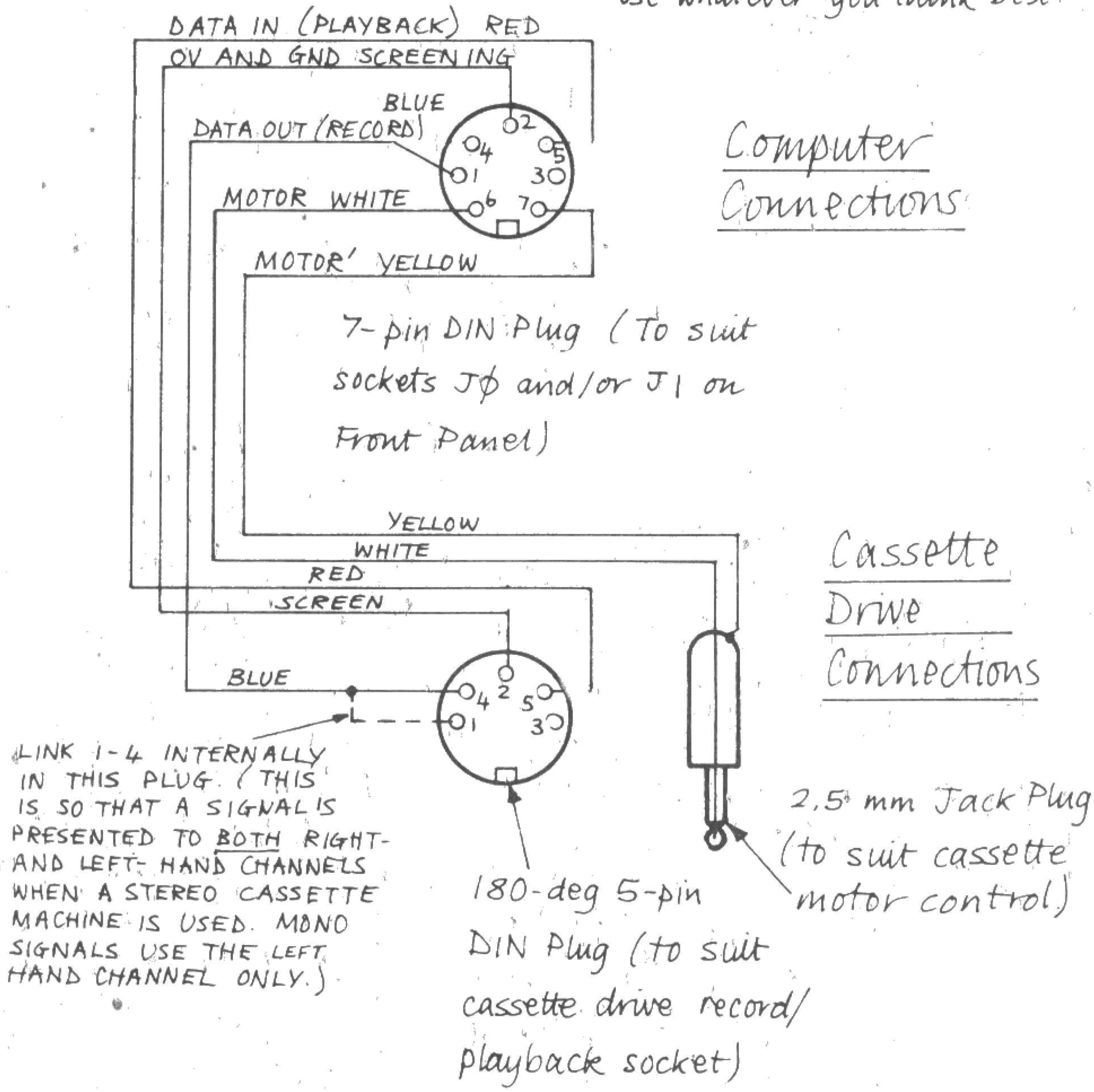
Drawn	D.M.P
Date	10-1-83
Scale	–

Interak

DTI-1

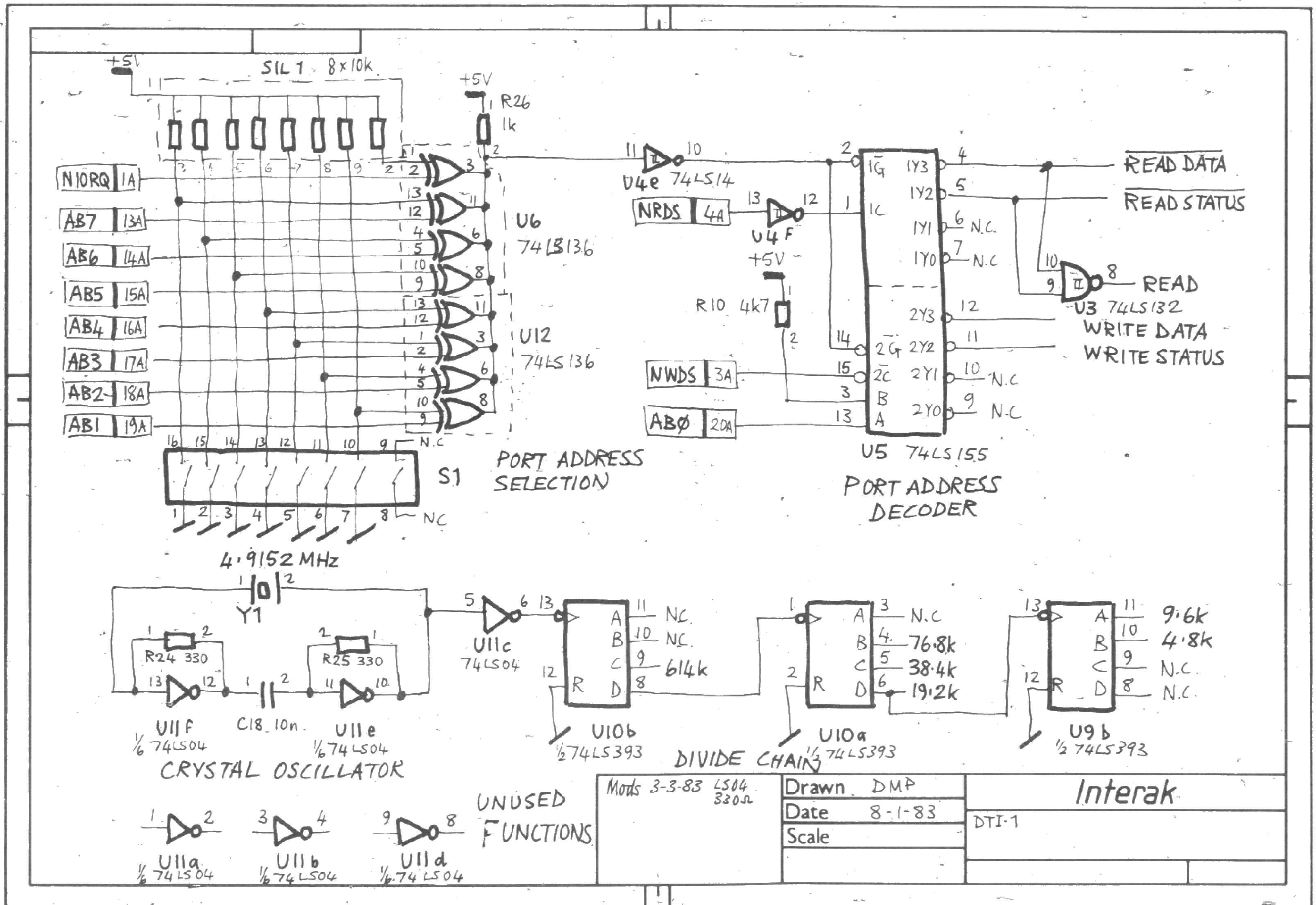
(VIEWS OF DIN PLUGS ARE WITH PINS AWAY FROM YOU)

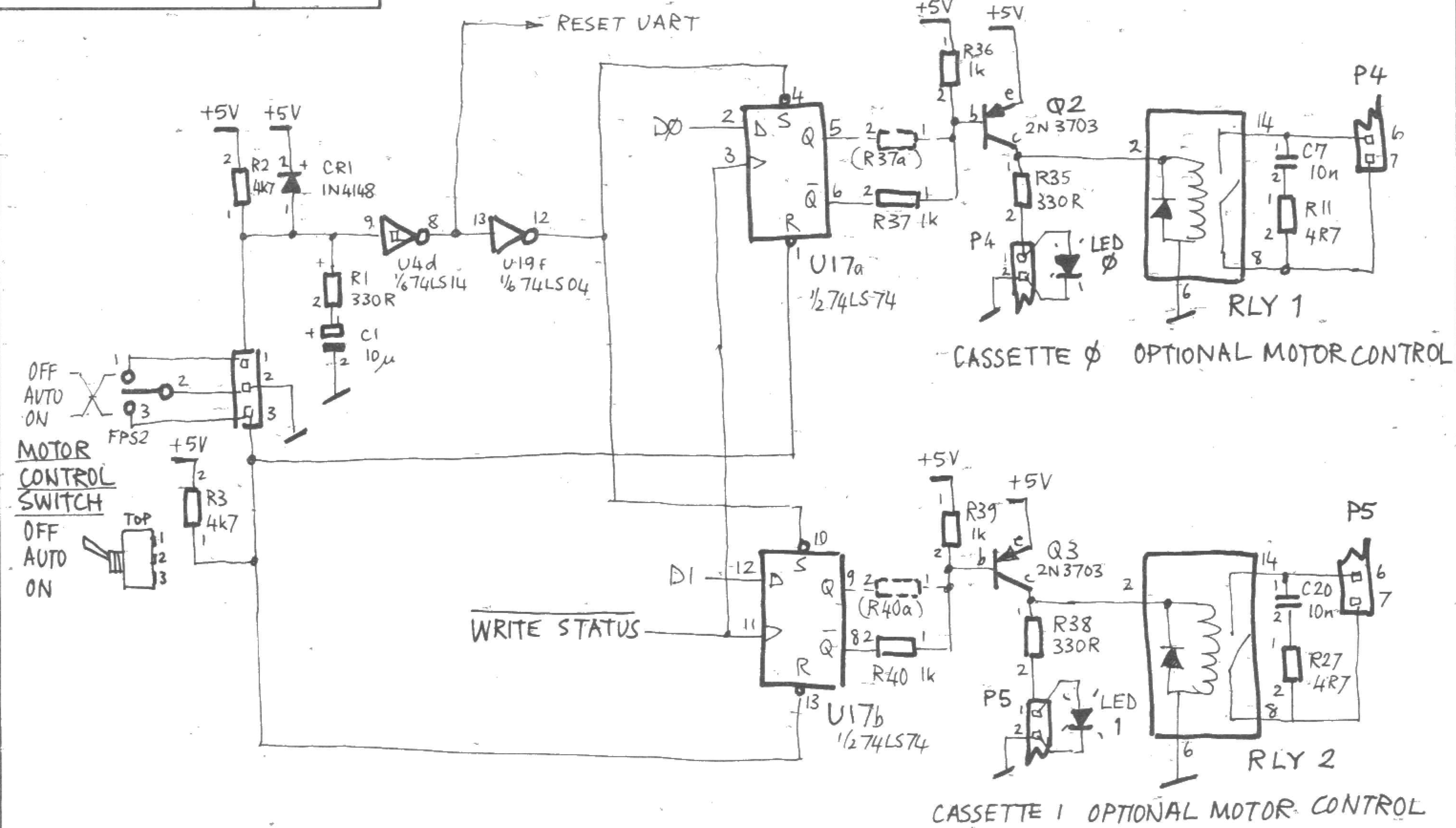
If the available cable does not have the specified colours, use whatever you think best.



Note: These connections may be varied to suit other cassette drives; this diagram gives typical connections only. If motor control is not required a standard 5-pin DIN to 5-pin DIN connector lead can be used.

Amended data out pin 3 Mar 84	Drwn D.M.P	**Greenbank Electronics**
	Date 18.3.82	DTI-1 CASSETTE CARD
	Scale –	TYPICAL CASSETTE DRIVE CONNECTIONS

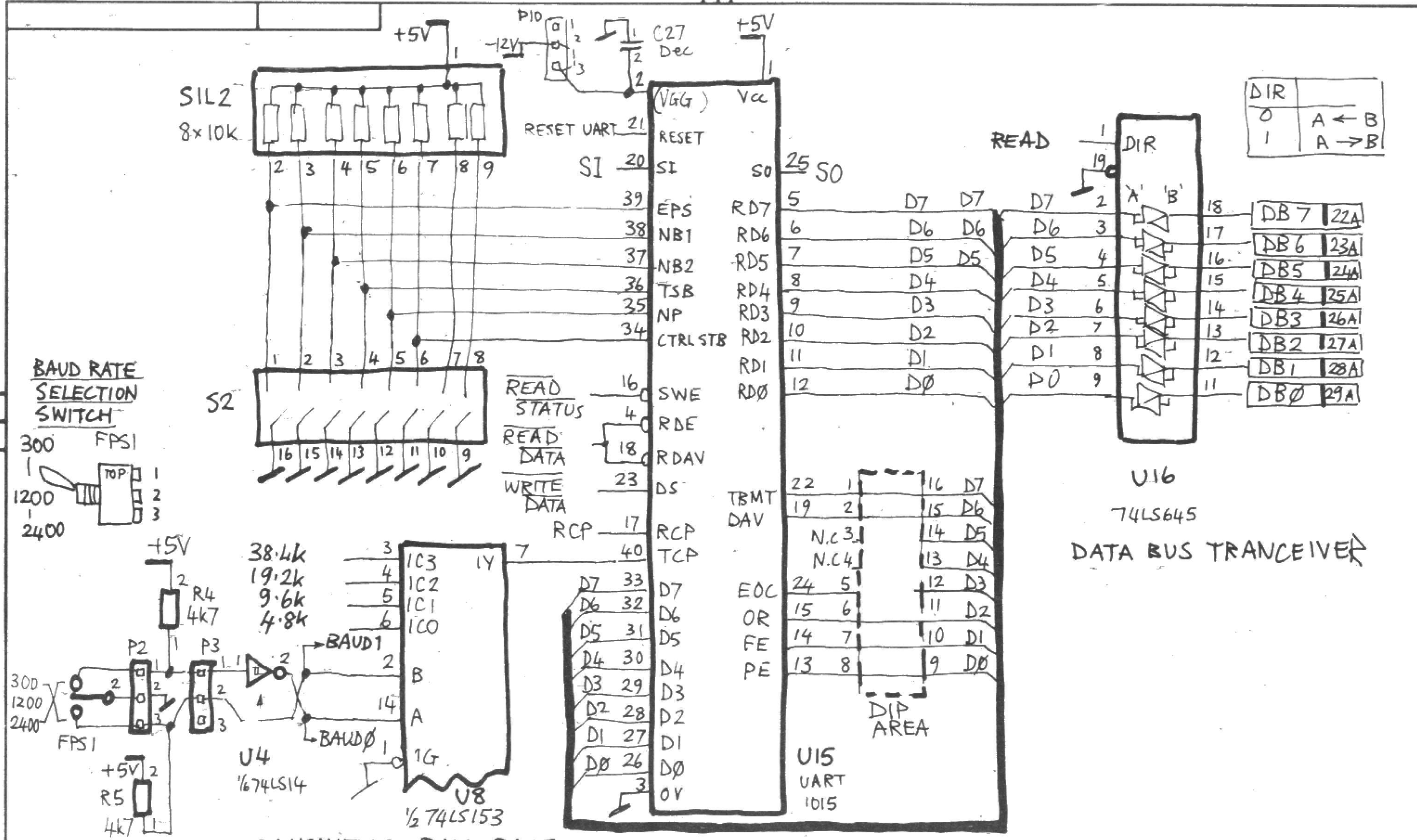

SIL 1 8x10k
+5V
R26 1k
N1ORQ 1A
AB7 13A
AB6 14A
AB5 15A
AB4 16A
AB3 17A
AB2 18A
AB1 19A
U6 74LS136
U12 74LS136
S1
PORT ADDRESS SELECTION
U4e 74LS14
NRDS 4A
U4F
R10 4k7
NWDS 3A
ABØ 20A
U5 74LS155
PORT ADDRESS DECODER
READ DATA
READ STATUS
READ
U3 74LS132
WRITE DATA
WRITE STATUS
N.C
4.9152 MHz
Y1
R24 330
R25 330
C18 10n
U11F 1/6 74LS04
U11e 1/6 74LS04
CRYSTAL OSCILLATOR
U11c 74LS04
U10b 1/2 74LS393
U10a 1/2 74LS393
U9b 1/2 74LS393
614k
76.8k
38.4k
19.2k
9.6k
4.8k
DIVIDE CHAIN
U11a 1/6 74LS04
U11b 1/6 74LS04
U11d 1/6 74LS04
UNUSED FUNCTIONS
Mods 3-3-83 LS04 330Ω
Drawn DMP
Date 8-1-83
Scale
Interak
DTI-1



Amended. R36, 35, NB Correct. Mar 84	
Drawn	DMP
Date	8-1-83
Scale	

Interak

DTI-1

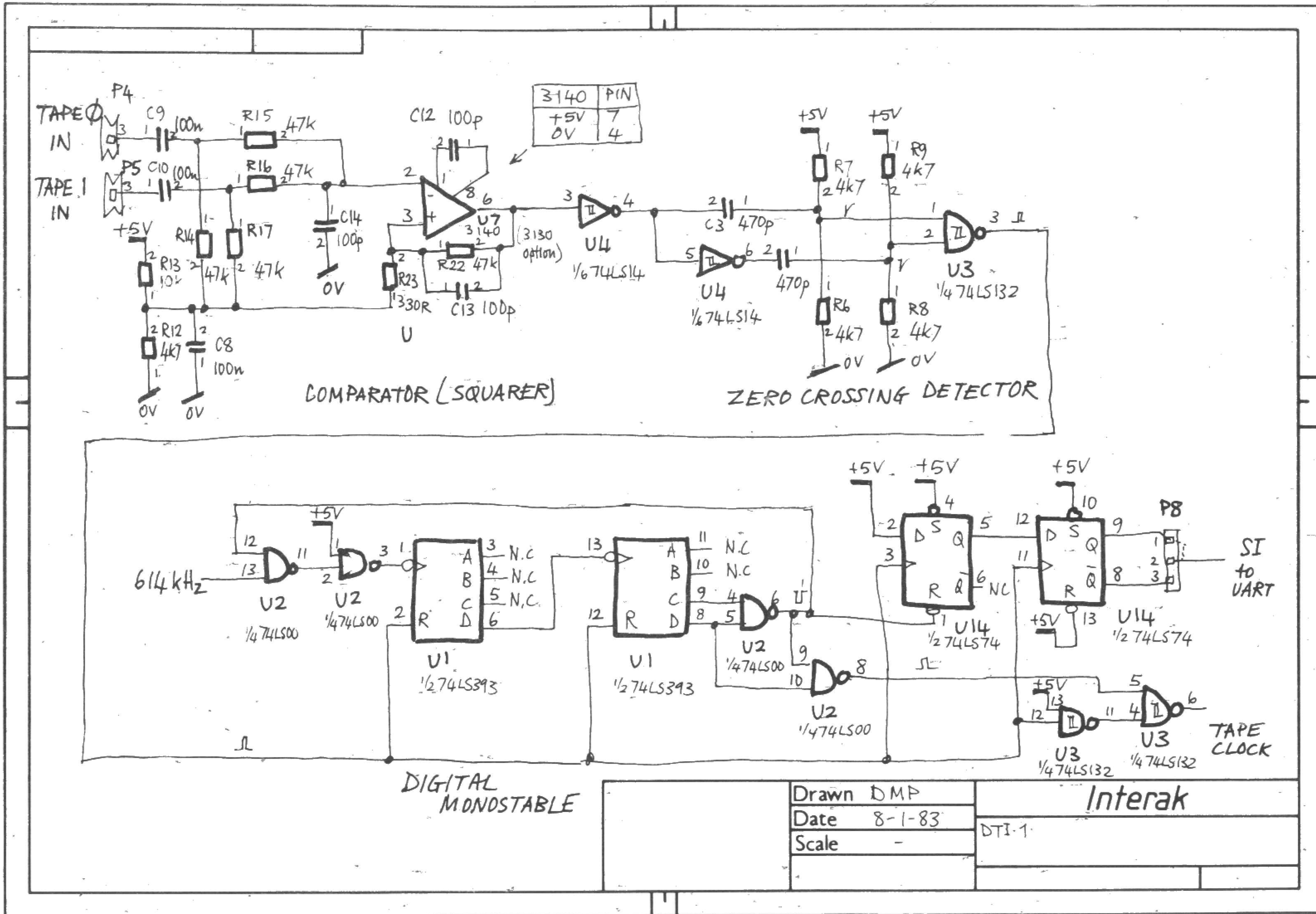


Mods 3-3-83 FPS1

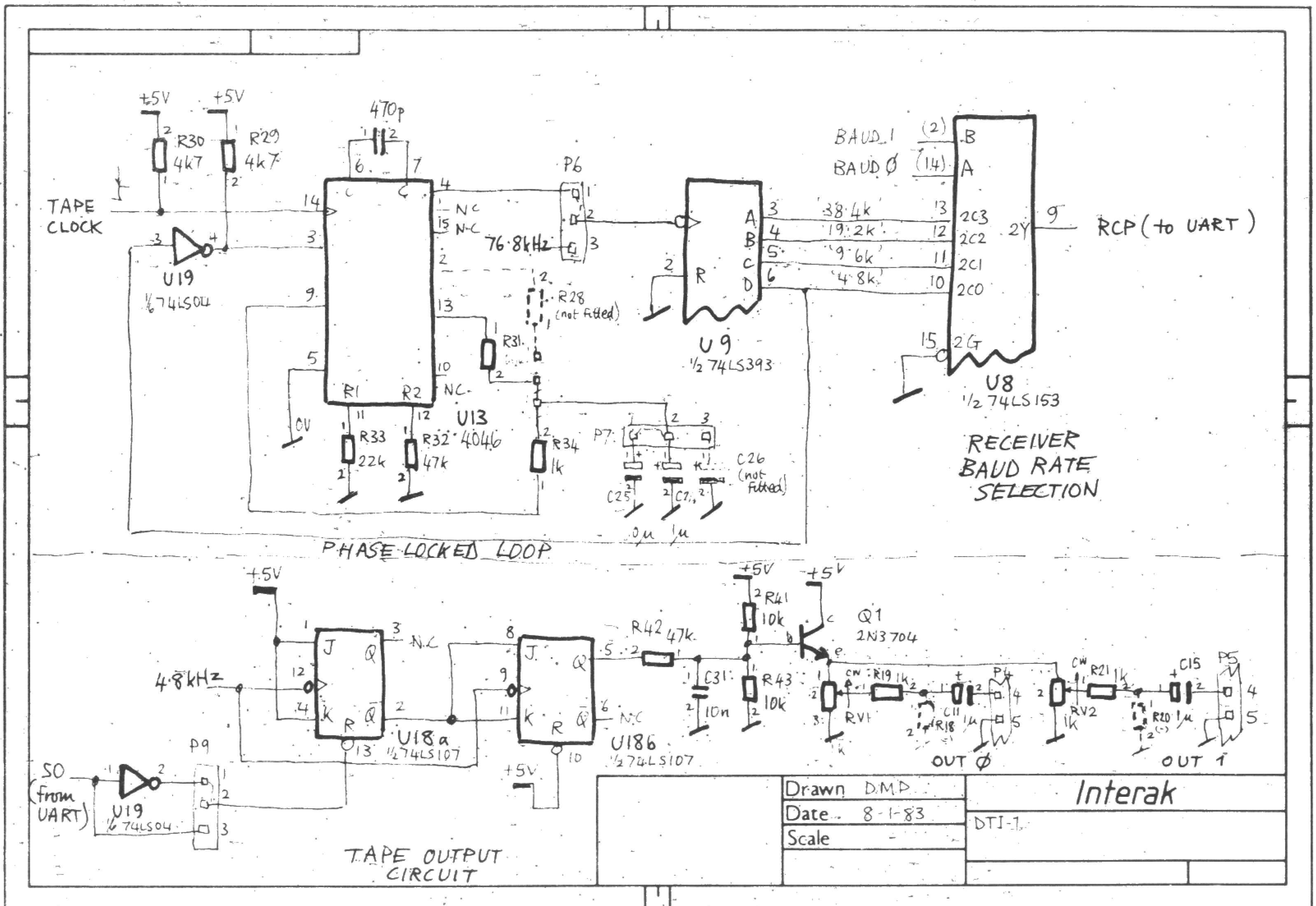
Drawn	DMP
Date	8-1-83
Scale	-

Interak

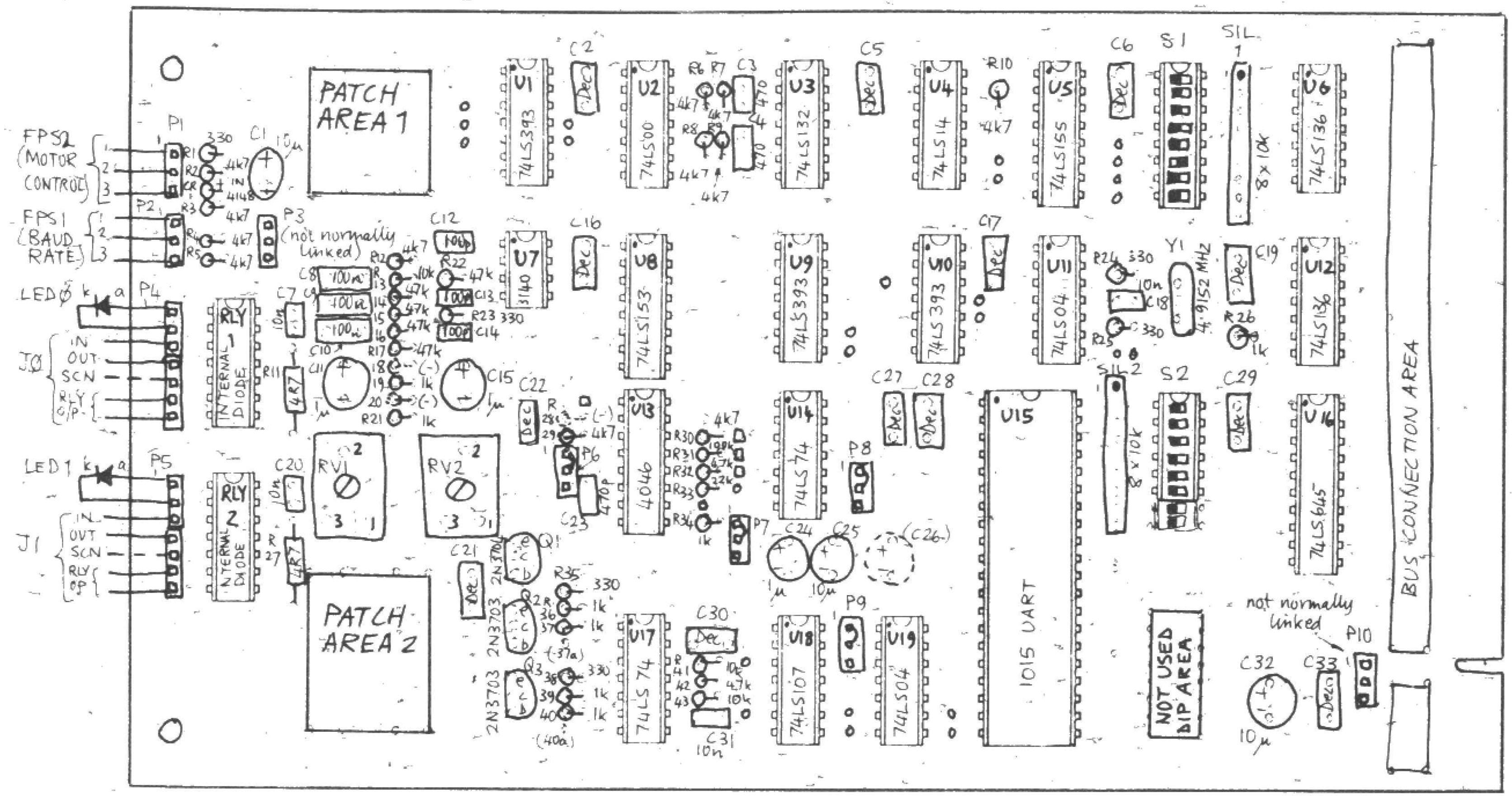
DTI-1



TAPE 0 IN
TAPE 1 IN
P4
P5
C9 100n
C10 100n
R15 47k
R16 47k
R14 47k
R17 47k
R13 10k
R12 4k7
C8 100n
C14 100p
C12 100p
U7 3140
(3130 option)
R22 47k
R23 330R
C13 100p
3140 PIN
+5V 7
0V 4
COMPARATOR (SQUARER)
U4 1/6 74LS14
C3 470p
470p
R7 4k7
R9 4k7
R6 4k7
R8 4k7
U3 1/4 74LS132
ZERO CROSSING DETECTOR
614kHz
U2 1/4 74LS00
U1 1/2 74LS393
N.C
U14 1/2 74LS74
NC
P8
SI to UART
TAPE CLOCK
DIGITAL MONOSTABLE
Drawn DMP
Date 8-1-83
Scale -
Interak
DTI-1



TAPE CLOCK
+5V
R30 4k7
R29 4k7
U19 1/6 74LS04
470p
U13 4046
R33 22k
R32 47k
R31
R28 (not fitted)
R34 1k
76·8kHz
P6
P7
C25
C27
C26 (not fitted)
0V
PHASE LOCKED LOOP
U9 1/2 74LS393
BAUD 1
BAUD Ø
38·4k
19·2k
9·6k
4·8k
U8 1/2 74LS153
RCP (to UART)
RECEIVER BAUD RATE SELECTION
4·8kHz
SO (from UART)
P9
U18a 1/2 74LS107
U18b 1/2 74LS107
R42 47k
C31 10n
R41 10k
R43 10k
Q1 2N3704
RV1
R19 1k
C11 1µ
R18
P4
OUT Ø
RV2 1k
R21 1k
C15 1µ
R20
P5
OUT 1
TAPE OUTPUT CIRCUIT
Drawn D.M.P.
Date 8-1-83
Scale -
Interak
DTI-1



Modified 3-3-83	Drawn D.M.P	**Greenbank Electronics**
	Date 3-6-82	DTI-1 COMPONENT OVERLAY
	Scale 1:1	

COMPONENT PARTS LIST FOR DTI-1 CARD

Issue 4

Date: March 1984

LISTED BY COMPONENT REFERENCE NUMBER

Resistors 0.25W (0.1" & 0.5" pitch)

R1	330R	0.1"	R23	330R	0.1"
R2	4k7	0.1"	R24	330R	0.1"
R3	4k7	0.1"	R25	330R	0.1"
R4	4k7	0.1"	R26	1k0	0.1"
R5	4k7	0.1"	R27	4R7	0.5"
R6	4k7	0.1"	R28	-	0.1"
R7	4k7	0.1"	R29	4k7	0.1"
R8	4k7	0.1"	R30	4k7	0.1"
R9	4k7	0.1"	R31	100k	0.1"
R10	4k7	0.1"	R32	47k	0.1"
R11	4R7	0.5"	R33	22k	0.1"
R12	4k7	0.1"	R34	1k0	0.1"
R13	10k	0.1"	R35	330R	0.1"
R14	47k	0.1"	R36	1k0	0.1"
R15	47k	0.1"	R37	1k0	0.1"
R16	47k	0.1"	R38	330R	0.1"
R17	47k	0.1"	R39	1k0	0.1"
R18	-	0.1"	R40	1k0	0.1"
R19	1k0	0.1"	R41	10k	0.1"
R20	-	0.1"	R42	47k	0.1"
R21	1k0	0.1"	R43	10k	0.1"
R22	47k	0.1"			

SIL Resistors (Use Sockets)

SIL1 9-pin 8x10k SIL2 9-pin 8x10k

Variable Resistor (Enclosed Min. Horiz.)

RV1 1k0 RV2 1k0

Capacitors

C1	10u	Al	0.2"	C18	10n	Cer	0.2"
C2	Dec		0.2"	C19	Dec		0.2"
C3	470p	Cer	0.2"	C20	10n	Cer	0.2"
C4	470p	Cer	0.2"	C21	Dec		0.2"
C5	Dec		0.2"	C22	Dec		0.2"
C6	Dec		0.2"	C23	470p	Cer	0.2"
C7	10n	Cer	0.2"	C24	1u0	Al	0.2"
C8	100n	Poly	0.2"	C25	10u	Al	0.2"
C9	100n	Poly	0.2"	C26	-		0.2"
C10	100n	Poly	0.2"	C27	Dec		0.2"
C11	1u0	Al	0.2"	C28	Dec		0.2"
C12	100p	Cer	0.2"	C29	Dec		0.2"
C13	100p	Cer	0.2"	C30	Dec		0.2"
C14	100p	Cer	0.2"	C31	10n	Cer	0.2"
C15	1u0	Al	0.2"	C32	10u	Al	0.2"
C16	Dec		0.2"	C33	Dec		0.2"
C17	Dec		0.2"				

LISTED BY COMPONENT VALUE

Resistors 0.25W

4R7	2	R11,27	(0.5")
330R	6	R1,23,24,25, 35,38	(0.1")
1k	8	R19,21,26,34, 36,37,38,39	(0.1")
4k7	12	R2-10,12,29, 30	(0.1")
10k	3	R13,41,43	(0.1")
22k	1	R33	(0.1")
47k	7	R14,15,16,17, 22,32,42	(0.1")
100k	1	R31	(0.1")
-	3	R18,20,28	(0.1")

("-" = not used)

SIL Resistors (Use Sockets)

9-pin 8x10k 2 SIL1,2

Variable Resistors (Enc Min Horiz)

1k 2 RV1,2

Capacitors

100p Cer	3	C12,13,14
470p Cer	3	C3,4,23
10n Cer	4	C7,18,20,31
Dec	13	C2,5,6,16,17,19,21, 22,27,28,29,30,33
100n Poly	3	C8,9,10
1u Al	3	C11,15,24
10u Al	3	C1,25,32
-	1	C26

"Al" = Low Leakage Min. Aluminium
"Cer" = Ceramic
"Dec" = 47-100n Decoupling grade polyester, or Ceramic
"Poly"= Polyester
"-" = Not used

COMPONENT PARTS LIST FOR DTI-1 CARD (continued)

LISTED BY COMPONENT REFERENCE NUMBER

Diodes

CR1	1N4148	0.1"
LED0	0.2" dia. (off card)	
LED1	0.2" dia. (off card)	

Transistors

Q1	2N3704/5
Q2	2N3702/3
Q3	2N3702/3

Quartz Crystal (0.2")

4.9152 MHz	1	Y1

Integrated Circuits (Use Sockets)

U1	74LS393	(14)	U11	74LS04	(14)
U2	74LS00	(14)	U12	74LS136	(14)
U3	74LS132	(14)	U13	4046	(16)
U4	74LS14	(14)	U14	74LS74	(14)
U5	74LS155	(16)	U15	1015	(40)
U6	74LS136	(14)	U16	74LS645	(20)
U7	3140	(8)	U17	74LS74	(14)
U8	74LS153	(16)	U18	74LS107	(14)
U9	74LS393	(14)	U19	74LS04	(14)
U10	74LS393	(14)			

DIL Switches (Use Sockets)

S1	16-pin 8xSPST
S2	16-pin 8xSPST

0.1" Pitch Pin Assemblies

P1	3-pin	P6	3-pin
P2	3-pin	P7	3-pin
P3	3-pin	P8	3-pin
P4	3-pin + 4-pin	P9	3-pin
P5	3-pin + 4-pin	P10	3-pin

Sundry

DIL and SIL Sockets, Switches, other hardware - see next page

LISTED BY COMPONENT VALUE

Diodes

1N4148	1	CR1 (0.5")
LED 0.2" dia.	2	LED0,1

Transistors

2N3702/3	2	Q2,3
2N3704/5	1	Q1

Quartz Crystal (0.2")

4.9152 MHz	1	Y1

Integrated Circuits (Use Sockets)

1015 UART	1	U15	(40 pin)
3140	1	U7	(8 pin)
4046	1	U13	(16 pin)
74LS00	1	U2	(14 pin)
74LS04	2	U11,19	(14 pin)
74LS14	1	U4	(14 pin)
74LS74	2	U14,17	(14 pin)
74LS107	1	U18	(14 pin)
74LS132	1	U3	(14 pin)
74LS136	2	U6,12	(14 pin)
74LS153	1	U8	(16 pin)
74LS155	1	U5	(16 pin)
74LS393	3	U1,9,10	(14 pin)
74LS645	1	U16	(20 pin)

DIL Switches (Use Sockets)

16-pin 8xSPST	2	S1,S2

0.1" Pitch Pin Assemblies

3 pin	10	P1-10
4 pin	2	P4',5'

Sundry

DIL and SIL Sockets, Switches, other hardware - see next page